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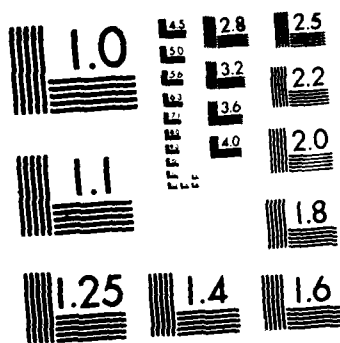
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Design History and Rationale. Naval Ocean Systems Center has investigated the potential of the systolic architecture for signal processing applications since the concept was introduced by H.T. Kung in 1978. This highly parallel architecture of nearest neighbor data communciation and repeated processing node structure promises a favorable marriage of VLSI wafer scale integration and matrix based signal processing algorithms. The successful merging of the technology with the mathematical concepts of eigenvector decomposition, single value decomposition, or orthogonal factorization necessitates a careful study of a large number of architectural issues. Functional factors associated with the design of a systolic processing element must be addressed. For instance, should bit-serial or bit parallel computation be utilized. Does the dynamic range of the candidate applications or numerical stability of the algorithms used require computations in fixed point and integer format or the architecturally more complex and slower floating point format. The relationship of input/output data flow rate and management and the internal computational speed must be studied in assessing the complexity of the processing element.

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HIGH-SPEED SYSTOLIC ARRAY TESTBED

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Design History And Rationale

Naval Ocean Systems Center has investigated the potential of the systolic architecture for signal processing applications since the concept was introduced by H.T. Kung in 1978[1]. This highly parallel architecture of nearest neighbor data communication and repeated processing node structure promises a favorable marriage of VLSI wafer scale integration and matrix based signal processing algorithms. The successful merging of the technology with the mathmatical concepts of eigenvector decomposition, single value decomposition, or orthogonal factorization necessitates a careful study of a large number of architectural issues. Functional factors associated with the design of a systolic processing element must be addressed. For instance, should bit-serial or bit parallel computation be utilized. Does the dynamic range of the candidate applications or numerical stability of the algorithms used require computations in fixed point and integer format or the architecturally more complex and slower floating point format. The relationship of input/output data flow rate and management and the internal computational speed must be studied in assessing the complexity of the processing element.

Design factors bearing on the type of systolic architecture used are also derived from the need to fully utilize each processing elements in the array. The number of elements, the interconnection scheme, the amount of local or global program intelligence must be established with consideration of the algorithm(s) to be mapped onto the architecture.

Initial work performed at NOSC[2] resulted in an 8 X 8 systolic array testbed and development software to aid in the subsequent algorithm mapping efforts. The array was built from off-the-shelf microprocessor based processor componentry. The architecture was very flexible and programmable and served as a good platform to address the design issues described earlier. The limited data input/output throughput structure and moderate clock speed of this testbed limited its usefulness for real-time signal processing applications.

NOSC is presently investigating the application of systolic architectures to adaptive beamforming. Using the background derived from the original testbed investigations and the performance requirements associated with a chosen beamforming algorithm, a second generation systolic array processor has been designed and built. A description of the algorithm, a special version of the modified Gram-Schmidt orthogonalizer, and its intended real-time adaptive beamforming application is beyond the scope of this paper. The architectural requirments imposed on the systolic array by the anticipated algorithm to be mapped, however, will be described here.

Testbed Architectural Features

The systolic array testbed system , figure 1, is composed of 16 Arithmetic Processing Modules (APM), 4 Input/Output Modules
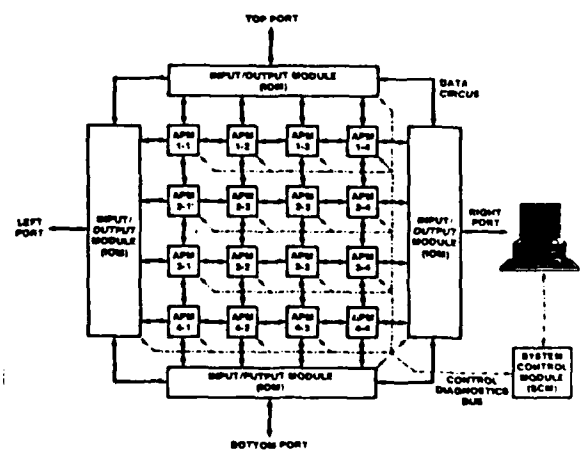

Figure 1 Systolic Testbed System

(IOM), a System Control Module (SCM), and the system host control computer (an IBM-AT for this initial configuration). The 16 APM's are systolically connected via orthogonal 40-bit bi-directional parallel data buses to adjacent APM's or to an IOM on each of the boundaries of the 4 X 4 square array. Data communication to hardware external to the array occur via the 4 external ports (top,bottom,right,and left). An additional 40-bit bus, called the data circus, is included in the processor architecture allowing the data movement around the periphery of the systolic array structure. Communication between the elements of the systolic array processing elements and the system control module is handled by a global bus called the Array Control Bus (ACB). The host computer communicates control, diagnostics and data to the APM's and IOM's via the SCM.

Arithmetic Processor Module
Functional Features

Each APM is composed of 330 off-the-shelf integrated circuits and has been constructed on a 16" X 16" wire wrap circuit panel. Figure 2 identifies the major functional components of each APM and hints to the highly parallel architecture contained within each module.
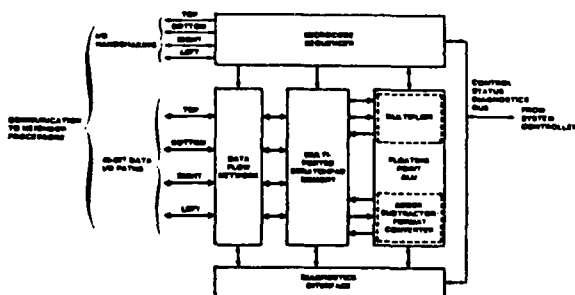

Figure 2   APM Functional Diagram

The computational power of the APM resides in the ALU which is composed of a pair of 8 MHz Weitek floating point processor chips, the 1033 multiplier and the 1032 ALU. The module architecture allows both of these chips to perform simultaneous computations on separate sets of operands while communication to neighboring processing modules may also occur. This degree of parallelism is achieved by the use of 4 Weitek register file chips (1066), which is a five ported 32 location 32-bit wide scratch pad memory. Because a total of 128 (4 X 32) locations for operand storage was deemed inadequate to

support most signal processing algorithms, an additional 4K locations of single ported memory is included in this scratch pad function.

The I/O structure of the APM has been made highly parallel and reconfigurable to allow the greatest latitude for algorithm data movement. Each register file chip can be dedicated to data movement associated with each adjacent module. This allows the simultaneous movement of up to four different data packets during a single transfer interval. The data transfer occur at the same rate as the internal computational rate, namely, 125 nanoseconds/transfer. The data flow network is capable of supporting a number of topological configurations. A characteristic of many signal processing algorithms is the need for some sort of global or broadcast data movement. Each APM can support broadcast in several different configurations. By moving data through the data flow network in a transparent mode, row, column and diagonal broadcasting is supported during a single clock cycle.

The on-board control of all the functional elements of the APM described so far originates from a micro-sequencer/instruction RAM. To accommodate the highly parallel nature of the APM, the instruction word contained in the RAM is 176 bits wide. The micro-sequencer accepts pointing vectors to the starting address of desired program segments via the control bus. The program flow can be modified by testing the I/O handshaking, the contents of the data tag byte, auxiliary mode registers, or data related arithmetic operations.

The final functional block in the APM is the diagnostics interface which allows the system host computer to load or interrogate APM memory registers and internal buses. This interface is used for such functions as down-loading instruction and data and has the additional feature of supporting initial debugging efforts and operational confidence testing/fault isolation.

Input/Output Module
Functional Features

Each IOM is composed of 190 integrated circuits and has been constructed on a 9" X 16" wire wrap circuit panel. Figure 3 identifies the major functional components of each of 4 IOM's in the system. To minimize the complexity of programming and the hardware debug cycle, the microcode sequencer and
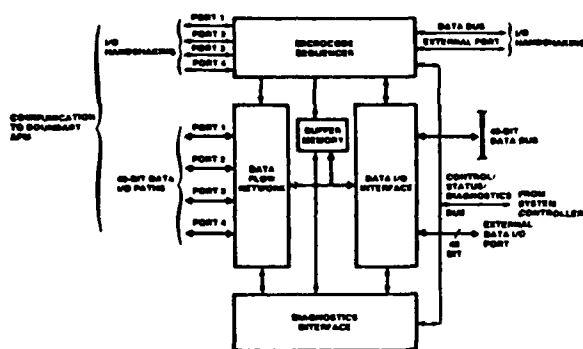
Figure 3 IOM Functional Diagram

Figure 4 SCM Functional Diagram

diagnostics interface are identical in function to those used in the APM. The IOM contains no data computational circuitry but is expressly designed to efficiently move data. The data flow network connects the data present at the boundary of the systolic array to the internal 4K buffer memory. The IOM handshaking and transfer rates are identical to the APM's th which it is connected. Each of the boundary IOM's has 2 non-systolic ports included which serve important interface funtions in the application of the array hardware. The external port comes complete with a separate set of handshaking signals which allow the intelligent communication of data with external hardware without interferring with the systolic movement of data within the array itself. The data bus (data circus) allows the IOM processors to act as a distributed interface system. The registration of data input and output to the array hardware with the external system hardware can be programmed into the IOM program.

System Control Module
Functional Features

The SCM is composed of 140 integrated circuits and is similar in construction to the IOM's. Figure 4 identifies its *functional components and its relationship* to the other system components. The main function of the SCM is to convert an extension of the host computer bus (16-bits) to a format used in the ACB (65-bits). The host computer can address each of the diagnostic and control registers contained in each or groups of APM's and/or IOM's. System status including global busy/ready, arithmetic error detection, or system instruction parity memory fault can be monitored by the host computer via the SCM. The incremental algorithm commands (the selection of the
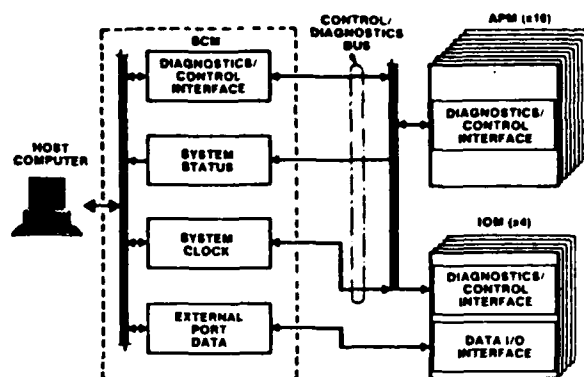
desired microcode program modules) can be directed at the hardware modules of the array. The system clock originates on the SCM board and a separate copy of the clock is sent to each system module. This clock is programmable in speed, and can be incrementally controlled and used during hardware debugging and algorithm mapping. The SCM incorporates the circuitry needed to allow data movement between the host computer and any one of the 4 external ports. This feature is included to aid in the initial mapping of the algorithm in the absence of the balance of the external system hardware.

Hardware Implementation Features

The system hardware, with the expection of the host computer, is housed in a 24" wide, 30" deep and 56" high equipment rack. A custom cardcage complete with fans was contructed which allows the mounting of the 16 APM cards in the front side of the backplane circuit card and the IOM's and SCM in the back. Due to the number of wide parallel buses and high clock speed of the array, all the systolic connectivity is contained in one 19" X 24" 10-layer circuit card. A special power distribution grid constructed from copper bar stock was attached to the backplane to accomodate the current load of the present system configuration (6500 ICs) and future enhancements up to 400 amps.

A secondary multibus cardcage has been included in the equipment cabinet to accomodate data acquisition system components and possible future use of a single board computer to replace the present IBM-AT host.

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